REMARKS

This application has been carefully reviewed in light of the Office Action dated January 12, 2007. Claims 1, 2, 4-14 and 16-22 remain in this application. Claims 1 and 5 are the independent Claims. Claim 9 has been amended. It is believed that no new matter is involved in the amendments or arguments presented herein. Reconsideration and entrance of the amendment in the application are respectfully requested.

Non-Art Based Rejections

Claim 9 was rejected under 35 U.S.C. § 112, for indefiniteness. In response, Claim 9 has been amended to depend from Claim 1. Reconsideration and withdrawal of the above § 112 rejections are respectfully requested.

Art-Based Rejections

Claims 1, 2, 5-9, 11-14 and 17-22 were rejected under 35 U.S.C. § 102(b) over U.S. Patent No. 5,822,559 (Narayan) in view of U.S. Patent No. 6,260,134 (Zuraski); Claims 4, 10 and 16 were rejected as obvious over Narayan in view of U.S. Patent Application Publication No. 2002/0056035 (Rozenshein).

Applicant respectfully traverses the rejections and submits that the claims herein are patentable in light of the clarifying amendments above and the arguments below.

The Narayan Reference

Narayan is directed to the alignment of variable byte length instructions to a plurality of decode units within a superscalar microprocessor. Narayan discloses an instruction prefix embedded in the head of an instruction code. The instruction prefix provides information regarding the operation to be performed. Early decode

units 207 perform partial decode of instructions conveyed by instruction alignment unit 206. Furthermore, early decode units 207 are configured to detect double dispatch instructions and then transfer double dispatch instructions to two of decode units 208. Register operands utilized by the double dispatch instruction are decoded and conveyed to reorder buffer 216 and register file 218 *(See Narayan; Col. 1, lines 66-67; Col. 16, lines 9-11; Col. 6, lines 47-49; Col. 6 line 59 – Col. 7, line 2).*

The Zuraski Reference

Zuraski is directed to a multiplexer 304 that shifts a fixed number of byte positions *(See Zuraski; Col. 13, line 65 – Col. 14, line 1).*

The Rozenshein Reference

Rozenshein is directed to an instruction system that includes an instruction root having an operation selection field for selecting an operation to be performed by a data processor and an instruction prefix *(See Rozenshein; Paragraph [0024]).*

The Claims are Patentable Over the Cited References

The present application is generally directed to a data processing device that performs pipeline control.

As defined by independent Claim 1, a data processing device which performs pipeline control includes a fetch circuit which fetches instruction codes of a plurality of instructions in instruction queues. The instructions include a given target instruction and a prefix instruction which precedes the target instruction and modifies a function of the target instruction. A prefix instruction decoder circuit performs decode processing only on a prefix instruction. The prefix instruction decoder circuit receives the instruction codes of the instructions before decoding that are fetched in the instruction queues, judges whether or not each of the

instruction codes is a given prefix instruction, and causes a target instruction modifying information register to store information necessary for decoding the target instruction modified by the prefix instruction when the judged instruction code is the given prefix instruction. A general-purpose decoder circuit receives each of the instruction codes of the instructions fetched in the instruction queues other than the prefix instruction as a decode instruction and decodes the decode instruction. When the decode instruction is the target instruction, the decoder circuit decodes the target instruction modified by the prefix instruction based on target instruction modifying information stored in the target instruction modifying information register. The given prefix instruction includes a shift prefix instruction for shifting an execution result of the target instruction, function of which is expanded by the prefix instruction. The prefix instruction decoder circuit causes the target instruction modifying information register to store shift information necessary for shifting the execution results of the target instruction modified by the shift prefix instruction when the input instruction code is the shift prefix instruction. The decoder circuit decodes the decode instruction so that the execution result of the target instruction modified by the shift prefix instruction are shifted based on the shift information stored in the target instruction modifying information register for execution of the target instruction when the decode instruction is the target instruction of the shift prefix instruction.

The applied references do not disclose or suggest the above features of the present invention as defined by independent Claim 1. In particular, the applied references do not disclose or suggest, "a prefix instruction which precedes the target instruction and modifies a function of the target instruction," as required by independent Claim 1.

As disclosed in column 16, lines 9-11, Narayan teaches an instruction prefix embedded in the head of an instruction code. Furthermore, the instruction prefix

"provides further information regarding the operation to be performed," *(See Narayan; Col. 1, lines 66-67).*

In contrast, the present invention requires a prefix instruction to precede the target instruction and to modify a function of the target instruction. Narayan does not modify the function of the target instruction.

Moreover, the applied references do not disclose or suggest, "a prefix instruction decoder circuit which performs decode processing only on a prefix instruction," as required by independent Claim 1.

Narayan discloses early decode units 207 that perform a partial decode of instructions conveyed by instruction alignment unit 206 *(See Narayan; Col. 6, lines 47-49).* In contrast, the present invention requires the prefix instruction decoder unit to perform decode processing only on a prefix instruction.

Moreover, the applied references do not disclose or suggest a prefix instruction decoder circuit that performs, "judging whether or not each of the instruction codes is a given prefix instruction," as required by independent Claim 1.

Narayan teaches early decode units 207 that are configured to detect double dispatch instructions and then transfer double dispatch instructions to two of decode units 208 *(See Narayan; Col. 6, lines 59-61).* Importantly, a double dispatch instruction executes two given instructions serially such that the first executed given instruction does not modify the subsequently executed given instruction.

In contrast, the prefix instruction decoder circuit of the present invention judges whether or not each of the instruction codes is a given prefix instruction. Narayan does not provide applicant's judging using the prefix instruction decoder circuit.

Furthermore, Applicant respectfully submits an inconsistency in the arguments presented by the Office. On page 4 of the Office Action, the instruction prefix embedded in the head of an instruction code is purported to correspond with

applicant's prefix instruction *(See Narayan; Col. 16, lines 9-11)*. However, on page 5 of the Office Action, Narayan's double dispatch instructions are alleged to correspond with the prefix instructions of the present invention *(See Narayan; Col. 6, lines 59-61)*.

Furthermore, the applied references do not disclose or suggest, "causing a target instruction modifying information register to store information necessary for decoding the target instruction modified by the prefix instruction," as required by independent Claim 1.

Narayan discloses decoding the register operands utilized by the double dispatch instruction and conveying the decoded operands to reorder buffer 216 and register file 218 *(See Narayan; Col. 6, line 61 – Col. 7, line 2)*. In contrast, the present invention requires a target modifying information register that stores information for decoding a target instruction modified by a prefix instruction. The ancillary references do not remedy the deficiencies of Narayan.

Moreover, the Office concedes that Narayan does not disclose or suggest, "the given prefix instruction includes a shift prefix instruction for shifting an execution result of the target instruction," as required by independent claim 1 Applicant respectfully submits that Zuraski is similarly deficient.

Zuraski merely teaches a multiplexer 304 that shifts a fixed number of byte positions *(See Zuraski; Col. 13, line 65 – Col. 14, line 1)*. In contrast, the present invention requires shifting of an execution result of the target instruction. The ancillary references do not remedy the deficiencies of Narayan and Zuraski.

Thus, Narayan and Zuraski, do not disclose or suggest these features of the present invention as required by independent Claim 1.

Since the applied references do not disclose or suggest the above features of the present invention as required by independent Claim 1, those references cannot

be said to anticipate nor render obvious the invention which is the subject matter of that claim.

Accordingly, independent Claim 1 is believed to be in condition for allowance and such allowance is respectfully requested.

Applicant respectfully submits that independent Claim 5 is allowable for at least the same reasons as discussed above in reference to independent Claim 1 and such allowance is respectfully requested.

The remaining claims depend either directly or indirectly from independent Claims 1 and 5 and recite additional features of the invention which are neither disclosed nor fairly suggested by the applied references and are also believed to be in condition for allowance and such allowance is respectfully requested.

Conclusion

Applicant believes the foregoing amendments comply with requirements of form and thus may be admitted under 37 C.F.R. § 1.116(b). Alternatively, if these amendments are deemed to touch the merits, admission is requested under 37 C.F.R. § 1.116(c). In this connection, these amendments were not earlier presented because they are in response to the matters pointed out for the first time in the Final Office Action.

Lastly, admission is requested under 37 C.F.R. § 1.116(b) as presenting rejected claims in better form for consideration on appeal.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los

Angeles, California telephone number (310) 785-4721 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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